In the Claims:

1. (Currently Amended) A semiconductor device comprising:

a dielectric layer;

a conductive line underlying the dielectric layer;

a via formed in the dielectric layer and extending into the conductive line to form a via recess in the conductive line, the via recess formed in the conductive line having a depth ~~of at least about 100 angstroms~~ between about 100 angstroms and about 600 angstroms; and

via-fill material filling the via recess and at least partially filling the via, such that the via-fill material is electrically connected to the conductive line.

2. (Original) The semiconductor device of claim 1, wherein the via-fill material comprises:

a barrier layer at least partially lining interior surfaces of the via recess and at least partially lining interior surfaces of the via; and

a conducting material, wherein the barrier layer is located between at least part of the conducting material and at least part of the dielectric layer.

3. (Original) The semiconductor device of claim 2, wherein the conducting material is electrically connected to the conductive line through the barrier layer.

4. (Original) The semiconductor device of claim 2, wherein the barrier layer comprises a material selected from a group consisting of tantalum, tantalum nitride, tungsten, compounds thereof, composites thereof, and combinations thereof.

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5. (Original) The semiconductor device of claim 2, wherein the conducting material comprises material selected from a group consisting of metal alloy, copper, copper alloy, aluminum, aluminum alloy, tungsten, poly-crystalline silicon, compounds thereof, composites thereof, and combinations thereof.

6. (Original) The semiconductor device of claim 5, wherein the depth of the via recess formed in the conductive line is between about 150 angstroms and about 300 angstroms.

7. (Original) The semiconductor device of claim 1, wherein the dielectric layer comprises:

a capped layer; and

a layer of insulating material overlying the capped layer.

8. (Original) The semiconductor device of claim 7, wherein the capped layer is a material comprising silicon-carbon having a thickness less than about 600 angstroms.

9. (Original) The semiconductor device of claim 8, wherein the capped layer has at least 30% carbon.

10. (Original) The semiconductor device of claim 7, wherein the capped layer comprises carbon-doped silicon nitride ($Si_xN_yC_z$).

11. (Original) The semiconductor device of claim 7, wherein the capped layer has a dielectric constant less than about 4.0.

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12. (Original) The semiconductor device of claim 7, wherein the capped layer has a thickness of less than about 600 angstroms.

13. (Original) The semiconductor device of claim 7, wherein the insulating material has a dielectric constant less than about 3.

14. (Original) The semiconductor device of claim 7, wherein the insulating material comprises a material selected from a group consisting of SiO_xC_y, FSG, Spin-On-Glass, Spin-On-Polymers, and combinations thereof.

15. (Original) The semiconductor device of claim 7, wherein the size of the via is less than about 900 angstroms.

16. (Original) The semiconductor device of claim 1, wherein the depth of the via recess formed in the conductive line is between about 150 angstroms and about 300 angstroms.

17. (Original) The semiconductor device of claim 1, wherein the depth of the via recess formed in the conductive line is between about 300 angstroms and about 600 angstroms.

18. (Original) The semiconductor device of claim 1, wherein the conductive line comprises a material selected from a group consisting of metal alloy, copper, aluminum, copper alloy, poly-crystalline silicon, metal silicide, compounds thereof, composites thereof, and combinations thereof.

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19. (Withdrawn) The semiconductor device of claim 1, wherein the dielectric layer has a dual damascene structure comprising another conductive line formed therein and being electrically connected to the conducting material in the via.

20. (Original) A semiconductor device comprising:

a dielectric layer comprising an insulating material layer and a capped layer, and the capped layer having a dielectric constant less than about 4;

a conductive line underlying the dielectric layer;

a via formed in the insulating material layer, through the capped layer, and extending into the conductive line to form a via recess in the conductive line, the via recess formed in the conductive line having a depth of in a range from about 100 angstroms to about 600 angstroms; and

via-fill material filling the via recess and at least partially filling the via, such that the via-fill material is electrically connected to the conductive line.

21. (Original) The semiconductor device of claim 20, wherein the conductive line is substantially made of copper.

22. (Original) The semiconductor device of claim 20, wherein the capped layer is made of material comprising silicon carbon and is located between the insulating material layer and the conductive line.

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23. (Original) A semiconductor device comprising:

a dielectric layer comprising an insulating material layer and a capped layer, and the capped layer comprising silicon and carbon;

a copper-based conductive line underlying the dielectric layer;

a via formed in the insulating material layer, through the capped layer, and extending into the conductive line to form a via recess in the conductive line, the via recess formed in the conductive line having a depth of in a range from about 100 angstroms to about 600 angstroms; and

via-fill material filling the via recess and at least partially filling the via, such that the via-fill material is electrically connected to the conductive line.

24. (Original) The semiconductor device of claim 23, wherein the capped layer comprises at least 30% carbon.

25. (Original) The semiconductor device of claim 23, wherein the size of the via is less than about 900 angstroms.

26. (Original) The semiconductor device of claim 23, wherein the depth of the via recess formed in the conductive line is between about 150 angstroms and 300 angstroms.

27. (Original) The semiconductor device of claim 23, wherein the depth of the via recess formed in teh conductive line is between about 300 angstroms and 600 angstroms.

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28. (Withdrawn) A method of fabricating a semiconductor device comprising:

forming a via in a dielectric layer and opening to a conductive line underlying the dielectric layer; and

forming a via recess in the conductive line at the via, the via recess in the conductive line having a depth ranging from about 100 angstroms to about 600 angstroms.

29. (Withdrawn) The method of claim 28, wherein the conductive line is substantially made of copper.

30. (Withdrawn) The method of claim 28, further comprising:

filling the via recess and at least partially filling the via with a via-fill material.

31. (Withdrawn) The method of claim 28, wherein the via-fill material comprises:

a barrier layer at least partially lining interior surfaces of the via recess and at least partially lining interior surfaces of the via; and

a conducting material, wherein the barrier layer is located between at least part of the conducting material and at least part of the dielectric layer.

32. (Withdrawn) The method of claim 28, wherein the dielectric layer comprises:

a capped layer; and

a layer of insulating material overlying the capped layer.

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33. (Withdrawn) The method of claim 28, wherein the size of the via is less than about 900 angstroms.

34. (Withdrawn) The method of claim 28, wherein the forming of the via recess includes a pre-metal cleaning process performed after the forming of the via.

35. (Withdrawn) The method of claim 34, wherein the pre-metal cleaning is a process selected from a group consisting of an argon sputter, an ammonia-based reactive process, a hydrogen-based reactive process, and combinations thereof.

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